Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 5, 7-9, 14 and 16 have been amended. Claim 18 is presently cancelled. Claims 4, 6 and 20-24 have been previously cancelled. Therefore, claims 1-3, 5, 7-17 and 19 are presented for examination.

35 U.S.C. §103(a) Rejection

Claims 1-3, 5, and 7-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomas et al. (U.S. Patent No. 5,752,011) in view of Shiell et al. (U.S. Patent No. 6,138,232). Applicants submit that the present claims are patentable over Thomas in view of Shiell.

Thomas discloses a method for controlling a processor's clock frequency so as to prevent overheating. The invention attempts to maximize the processing speed of the processor while preventing overheating. In a preferred embodiment, the invention monitors a processor's activity and its temperature. When there is no activity for the processor, a slowed clock frequency is used, thereby saving power and lowering the thermal heat produced by the processor. When there is activity for the processor, a fast clock frequency is used. However, when prolonged activity (i.e., sustained fast clock frequency) causes the processor's temperature to become dangerously high for proper operation, the clock frequency is reduced so as to maintain processing speed at a reduced speed while preventing overheating. See Thomas at Abstract.

Shiell discloses a method of operating a microprocessor. The microprocessor accepts an interrupt from one of a plurality of interrupt sources. The microprocessor then operates at a rate dependent upon the interrupt source. The rate of power consumption by

the microprocessor corresponds to the selected rate of instruction operation. A rate table stores a table of interrupt source to rate of instruction operation. The rate table is accessed upon receipt of an interrupt to obtain a rate of instruction operation corresponding to the interrupt source. The microprocessor is then operated at the recalled rate. The rate table may be a read only memory or a read/write memory loaded upon initiation of the microprocessor. The rate of instruction operation may be controlled by a rate of instruction dispatch. For a superscalar microprocessor capable of concurrently executing plural instructions simultaneously the rate of instruction operation may be set by setting a number of instructions dispatched per instruction cycle. This could include dispatching instructions to a number of execution units based upon the selected rate. Electric power consumption is conserved by powering only those execution units to which instructions are dispatched. See Shiell at col. 1, ll. 45 – col. 2, ll. 25.

Claim 1 recites:

> A system comprising:
> a central processing unit (CPU) including power management logic to enable the CPU to execute a first quantity of instructions per cycle whenever the temperature of the CPU exceeds a predetermined threshold and to execute a second quantity of instructions per cycle whenever the temperature of the CPU is below the predetermined threshold, wherein the power management logic includes an artificial activity generator to generate artificial activity within the CPU to minimize current spikes within the CPU; and
> programmable array logic (PAL) to operate as an interrupt handler to control the CPU upon receiving an interrupt.

Applicants submit that neither Thomas nor Shiell disclose or suggest an artificial activity generator to generate artificial activity within the CPU to minimize current spikes

within the CPU, as recited by claim 1. Thomas discloses a method for controlling a processor's clock frequency so as to prevent overheating. (Abstract). However, nowhere does Thomas disclose or suggest an artificial activity generator to generate artificial activity within the CPU to minimize current spikes within the CPU. Shiell discloses a method for conserving power when operating a microprocessor. (Abstract). Nonetheless, nowhere does Shiell disclose or suggest an artificial activity generator to generate artificial activity within the CPU to minimize current spikes within the CPU. Accordingly, Thomas and Shiell, individually or in combination, do not disclose or suggest an artificial activity generator to generate artificial activity within the CPU to minimize current spikes within the CPU. Therefore, claim 1 is patentable over Thomas in view of Shiell.

Claims 2-3, 5 and 7 depend from claim 1 and include additional features. Therefore, claims 2-3, 5 and 7 are also patentable over Thomas in view of Shiell.

Claims 8 and 16 include features similar to those recited in claim 1, namely, entering an artificial activity mode to generate artificial activity within the CPU to minimize current spikes within the CPU. Therefore, applicants submit that claims 8 and 16 are patentable over Thomas in view of Shiell, for the reasons stated above with respect to claim 1. Claims 9-15 and 17 and 19 depend from claims 8 and 16, respectively. As a result, claims 9-15 and 17 and 19 are also patentable over Thomas in view of Shiell.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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